ABSTRACT OF THE INVENTION

A stacked multichip package (100) has a base carrier (102) having a top side (108) and a bottom side (110), a bottom integrated circuit die (104) having a bottom surface (112) attached to the base carrier top side (108), and an opposing, top surface (114). The top surface (114) has a peripheral area including a plurality of first bonding pads and a central area (120). A bead (124) is formed on the top surface (114) of the bottom die (104) between the peripheral area and the central area (120). A top integrated circuit die (106) having a bottom surface is positioned over the bottom die (104) and the bottom surface of the top die (106) is attached to the top surface (114) of the bottom die (104) via the bead (124). The bead (124) maintains a predetermined spacing between the bottom die (104) and the top die (106) so that wirebonds of first wires (122) connecting the bottom die (104) to the base carrier (102) are not damaged when the top die (106) is attached to the bottom die (104).